Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E. SCANNED ___ Q.A. ___	PATENT DATE

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/916598		~~365~~ 710		~~2818~~ ~~2181~~ 2112	

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TITLE
Cache coherent split transaction memory bus architecture and protocol for a multi processor chip device

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ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION								
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☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to ____________ (date) has been disclaimed.	(Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ____________	(Primary Examiner) (Date)			ISSUE FEE	
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